

FIG. 1

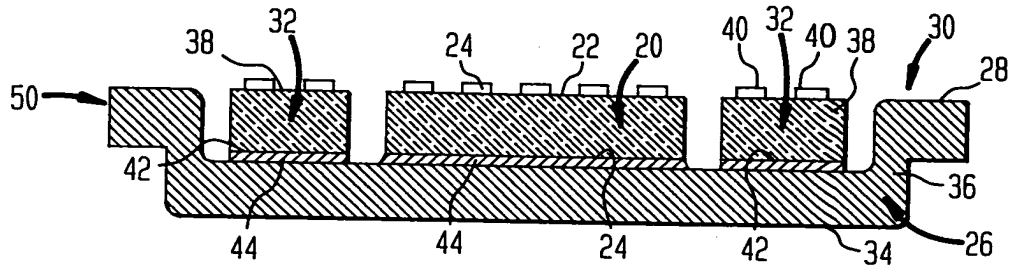


FIG. 2

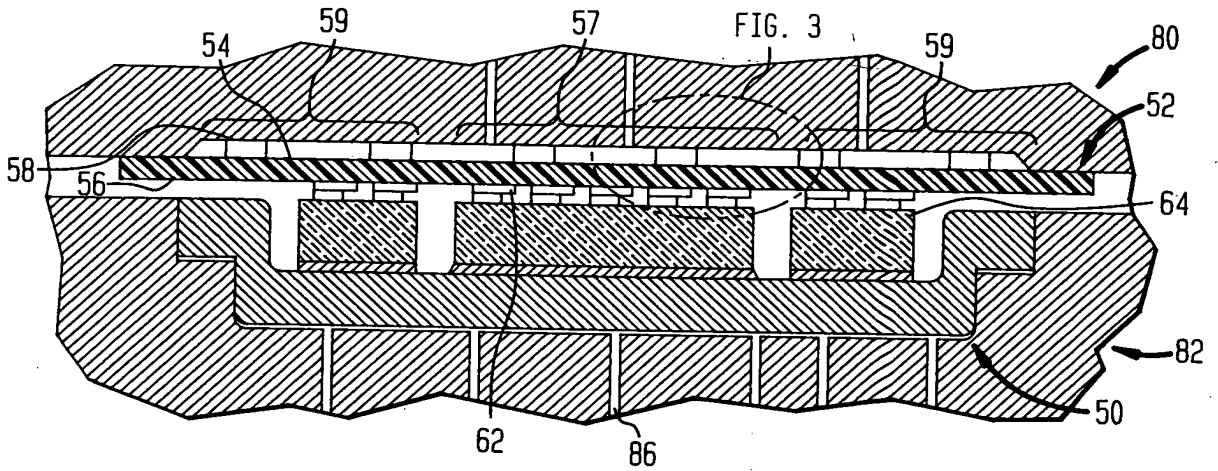


FIG. 3

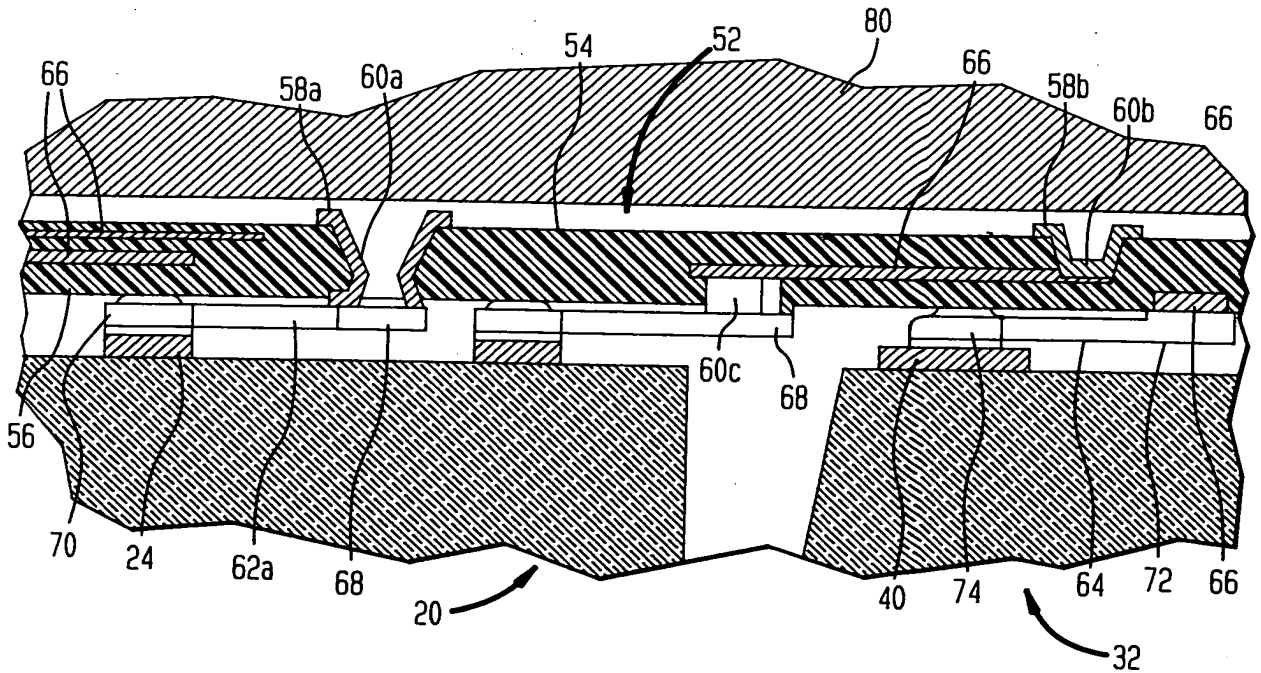


FIG. 4

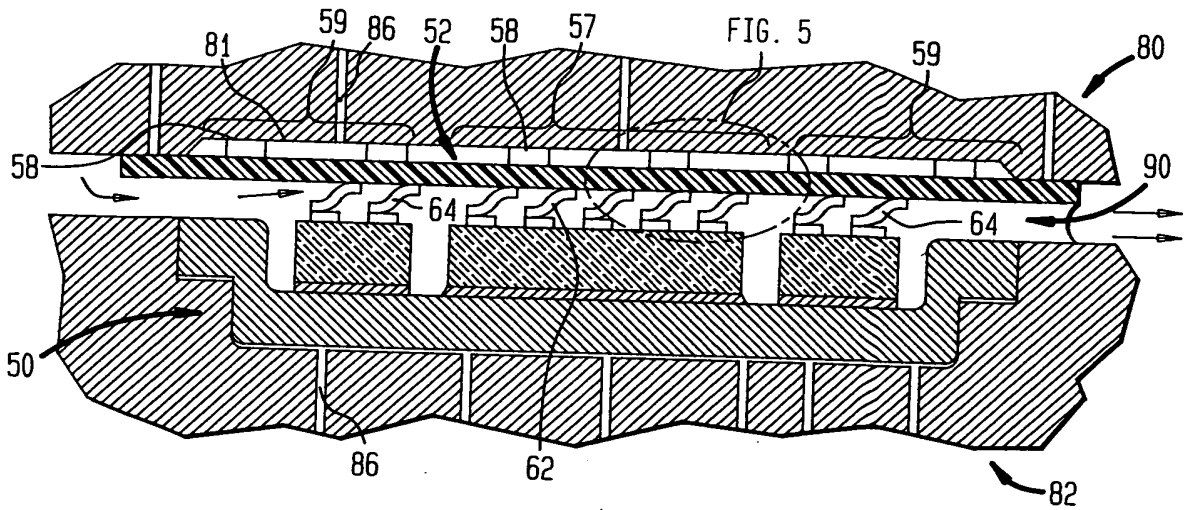
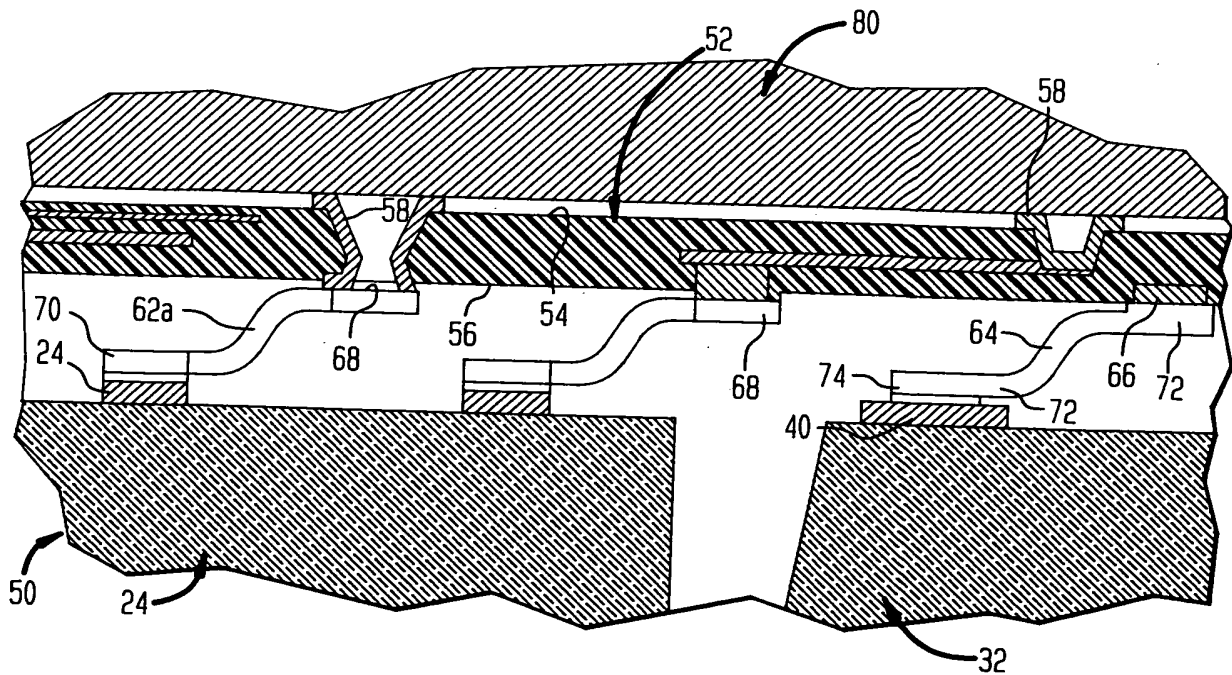


FIG. 5



A cross-sectional view of a semiconductor device assembly. The assembly includes a substrate 96 with a series of solder bumps 98. A layer 57 is formed on the substrate, containing openings 59. A layer 58 is formed on top of layer 57. A layer 94 is formed on top of layer 58. A series of solder bumps 52 are formed on layer 94, connecting it to a series of solder bumps 28. A layer 38 is formed on top of layer 94, containing openings 38. A layer 20 is formed on top of layer 38, containing openings 20. A layer 22 is formed on top of layer 20, containing openings 22. A layer 50 is formed on top of layer 22, containing openings 50.

FIG. 8

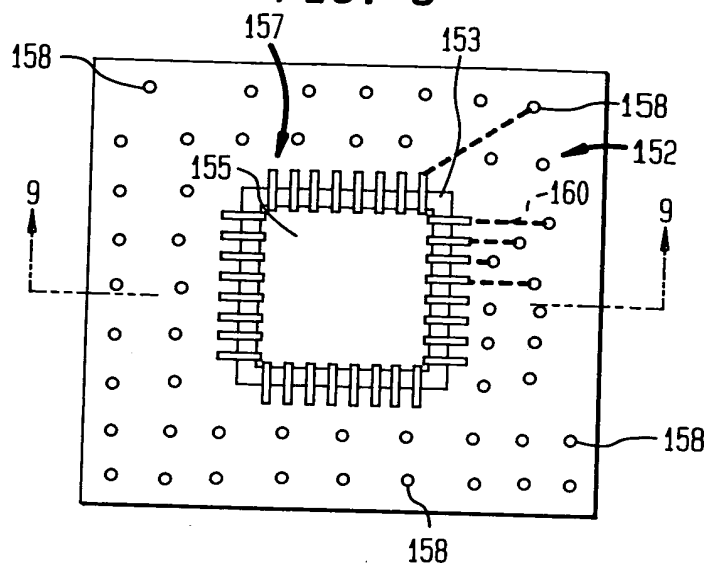


FIG. 9

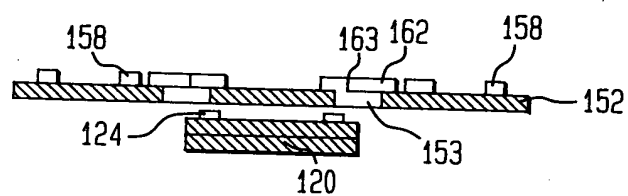


FIG. 10

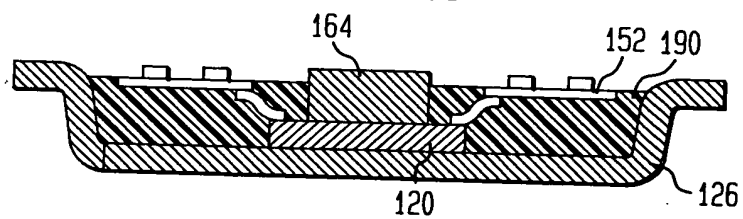


FIG. 11

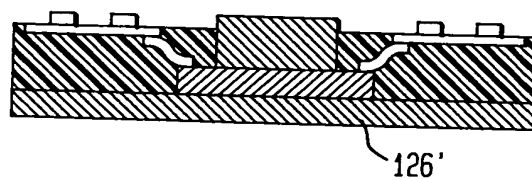


FIG. 12

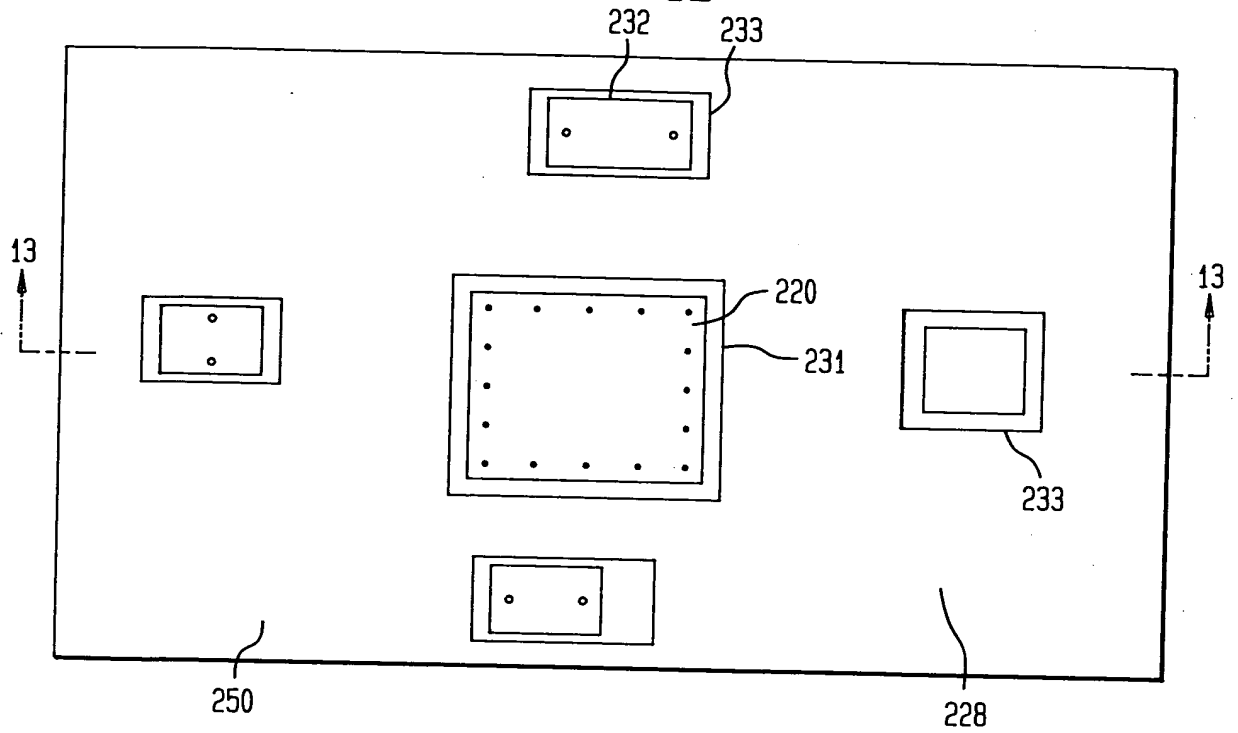


FIG. 13

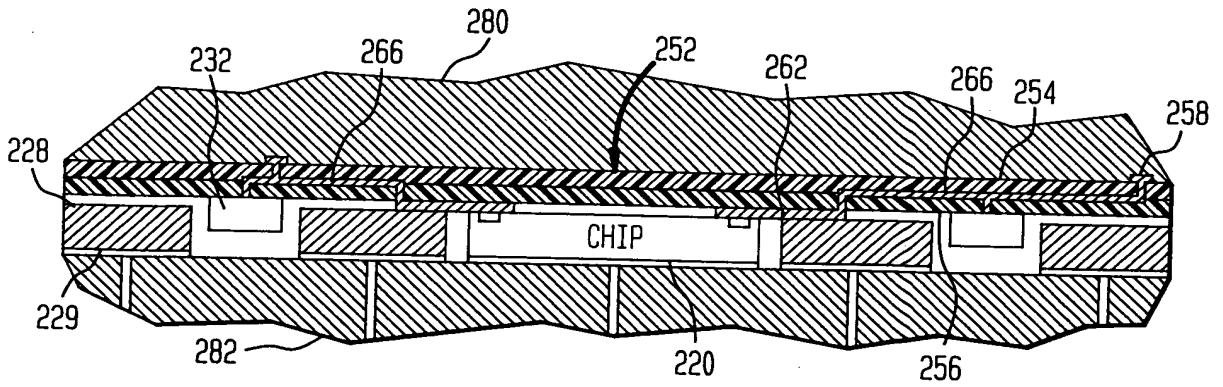


FIG. 14

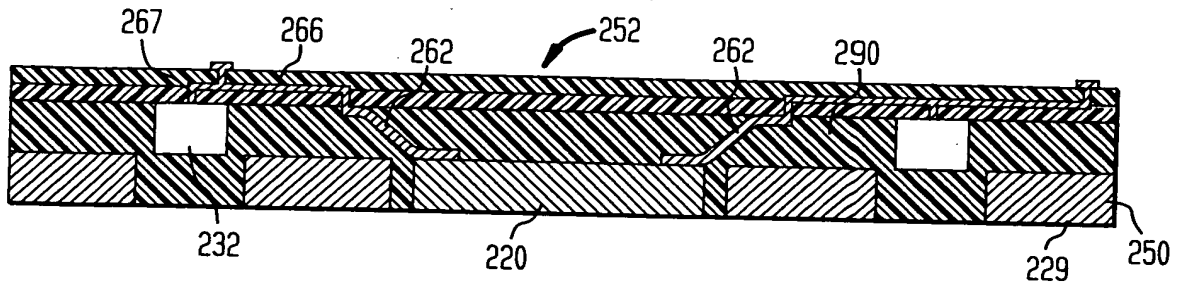


FIG. 15

